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10/609,215	06/26/2003	Albert F. Winkeler III	66638/40337	6484

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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/609,215	WINKELER ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-14,16-22,26-34 and 36-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-22,25-33 and 54-62* is/are allowed.

6)☒ Claim(s) *1-8,10-11,13-14,16-19,34,36-37,47-53, and 63-66* is/are rejected.

7)☒ Claim(s) *12 and 38-46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 3, 34, 36, 37, 50, 51, 63, 65, and 66 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 4,443,850 to Harris ("Harris").

3. In reference to Claim 1, Harris discloses a data processing apparatus comprising: a plurality of data processing boards (See Figure 1 Numbers 300a-300d); a bus connecting the boards with each other (See Figure 1); and each board comprising a communication utility for communicating data over the bus to another board through a plurality of channels, and wherein at least one of the channels has a user-redefinable configuration, the user-redefinable configuration including whether direct memory access is used or not used to transfer data over the bus (See Column 47 Lines 3-25).

4. In reference to Claim 2, Harris discloses the limitations as applied to Claim 1 above. Harris further discloses that each channel is separately user-redefinable (See Column 47 Lines 3-25).

5. In reference to Claim 3, Harris discloses the limitations as applied to Claim 1 above. Harris further discloses that the at least one channel configuration is user-redefinable with one of a plurality of available configuration types (See Column 47 Lines 3-25).

6. Claim 34, 63, 65, and 66 recite limitations which are substantially equivalent to those of Claim 1, and are rejected under similar reasoning.

7. In reference to Claim 36, Harris discloses the limitations as applied to Claim 35 above. Harris further discloses that the defining step comprises defining a plurality of redefinable communication channel configurations for a plurality of channels through which data is communicated by the communication utility (See Column 47 Lines 3-25).

8. In reference to Claim 37, Harris discloses the limitations as applied to Claim 36 above. Harris further discloses that the defining step comprises selecting a configuration type for each channel from a plurality of available configuration types (See Column 47 Lines 3-25).

9. In reference to Claim 50, Harris discloses the limitations as applied to Claim 36 above. Harris further discloses that the defining step further comprises defining the

conditions under which a channel uses a DMA data transfer (See Column 47 Lines 3-25).

10. In reference to Claim 51, Harris discloses the limitations as applied to Claim 36 above. Harris further discloses that the defining step comprises defining the number of channels through which data is communicated (See Column 47 Lines 3-25).

11. Claims 1, 2, 3, 34, 36, 37, 50, 51, 63, 65, and 66 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 4,837,677 to Burrus, Jr. et al. ("Burrus").

12. In reference to Claim 1, Burrus discloses a data processing apparatus comprising: a plurality of data processing boards (See Figure 1 Number 1); a bus connecting the boards with each other (See Figure 1 '+USART DATA' and '+SYSTEM DATA BUS'); and each board comprising a communication utility for communicating data over the bus to another board through a plurality of channels, and wherein at least one of the channels has a user-redefinable configuration, the user-redefinable configuration including whether direct memory access is used or not used to transfer data over the bus (See Column 3 Line 53 – Column 4 Line 8 and Column 4 Lines 28-41).

13. In reference to Claim 2, Burrus discloses the limitations as applied to Claim 1 above. Burrus further discloses that each channel is separately user-redefinable (See Column 4 Lines 28-33).

14. In reference to Claim 3, Burrus discloses the limitations as applied to Claim 1 above. Burrus further discloses that the at least one channel configuration is user-redefinable with one of a plurality of available configuration types (See Column 4 Lines 28-41).

15. Claim 34, 63, 65, and 66 recite limitations which are substantially equivalent to those of Claim 1, and are rejected under similar reasoning.

16. In reference to Claim 36, Burrus discloses the limitations as applied to Claim 35 above. Burrus further discloses that the defining step comprises defining a plurality of redefinable communication channel configurations for a plurality of channels through which data is communicated by the communication utility (See Column 4 Lines 28-33).

17. In reference to Claim 37, Burrus discloses the limitations as applied to Claim 36 above. Burrus further discloses that the defining step comprises selecting a configuration type for each channel from a plurality of available configuration types (See Column 4 Lines 28-33).

18. In reference to Claim 47, Burrus discloses the limitations as applied to Claim 36 above. Burrus further discloses that defining a configuration comprises selecting a maximum data transfer size for a channel (See Column 24 Lines 5-22).

19. In reference to Claim 50, Burrus discloses the limitations as applied to Claim 36 above. Burrus further discloses that the defining step further comprises defining the conditions under which a channel uses a DMA data transfer (See Column 4 Lines 28-41).

20. In reference to Claim 51, Burrus discloses the limitations as applied to Claim 36 above. Harris further discloses that the defining step comprises defining the number of channels through which data is communicated (See Column 4 Lines 28-41).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 4, 5, 6, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burrus as applied to Claim 1 above, and further in view of The Free On-Line Dictionary of Computing ("FOLDOC").

23. In reference to Claim 4, Burrus discloses the limitations as applied to Claim 1 above. Burrus does not disclose that the boards are VME boards and the bus is a VME bus. FOLDOC discloses the use of a VME bus and boards (See entries 'VMEbus' and 'Versa Module Europa').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Burrus with a VME bus and boards, resulting in the invention of Claim 4, because VME is a standardized bus that is widely used (See entry 'VMEbus' in FOLDOC) and has become a popular protocol in the computer industry (See entry 'Versa Module Europa' in FOLDOC).

24. In reference to Claim 5, Burrus and FOLDOC disclose the limitations as applied to Claim 4 above. Burrus further discloses that the channel configuration is user-redefinable with respect to a maximum data transfer size for the channel (See Column 24 Lines 5-22) and the conditions under which DMA is used by the channel for data transfers across the bus (See Column 4 Lines 28-41).

25. In reference to Claim 6, Burrus and FOLDOC disclose the limitations as applied to Claim 4 above. Burrus further discloses that the communication utility is redefinable

with respect to the number of channels through which data is communicated, the number of channels defined by at least one user input (See Column 3 Line 53 – Column 4 Line 8 and Column 4 Lines 28-41).

26. Claim 52 recites limitations which are substantially equivalent to those of Claim 4, and are rejected under similar reasoning.

27. Claims 7, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris.

28. In reference to Claim 7, Harris discloses a data processing apparatus comprising: first and second data processing boards (See Figure 1 Numbers 300a-300d); a bus connecting the boards with each other (See Figure 1); and each board comprising a communication utility for communicating data according to a redefinable configuration, the communication utility being configured to communicate data through a plurality of channels, and at least one channel has a user-redefinable configuration with respect to whether DMA is used or not used to transfer data over the bus (See Column 47 Lines 3-25). Harris does not expressly disclose that a bus utilization percentage in a range from 13% to 25% is achieved for 8 Kbyte data transfers across the bus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to achieve an 8Kbyte data transfer with 13%-25% bus utilization in the device of Harris, resulting in the invention of Claim 7, because Applicant has not

disclosed that the bus claimed bus utilization provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected the device disclosed by Harris to operate equally well with the claimed bus utilization percentage as with another bus utilization percentage. Therefore, it would have been obvious to one of ordinary skill in the art to modify the device of Harris to obtain the invention as specified in Claim 7.

29. In reference to Claim 10, Harris discloses the limitations as applied to Claim 7 above. Harris further discloses that each channel is separately user-redefinable (See Column 47 Lines 3-25).

30. In reference to Claim 11, Harris discloses the limitations as applied to Claim 7 above. Harris further discloses that the at least one channel configuration is user-redefinable with one of a plurality of available configuration types (See Column 47 Lines 3-25).

31. Claims 7, 10, 11, 13, 16, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burrus.

32. In reference to Claim 7, Burrus discloses a data processing apparatus comprising: first and second data processing boards (See Figure 1 Number 1); a bus connecting the boards with each other (See Figure 1 '+USART DATA' and '+SYSTEM

DATA BUS'); and each board comprising a communication utility for communicating data according to a redefinable configuration, the communication utility being configured to communicate data through a plurality of channels, and at least one channel has a user-redefinable configuration with respect to whether DMA is used or not used to transfer data over the bus (See Column 3 Line 53 – Column 4 Line 8 and Column 4 Lines 28-41). Burrus does not expressly disclose that a bus utilization percentage in a range from 13% to 25% is achieved for 8 Kbyte data transfers across the bus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to achieve an 8Kbyte data transfer with 13%-25% bus utilization in the device of Burrus, resulting in the invention of Claim 7, because Applicant has not disclosed that the bus claimed bus utilization provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected the device disclosed by Burrus to operate equally well with the claimed bus utilization percentage as with another bus utilization percentage. Therefore, it would have been obvious to one of ordinary skill in the art to modify the device of Burrus to obtain the invention as specified in Claim 7.

33. In reference to Claim 10, Burrus discloses the limitations as applied to Claim 7 above. Burrus further discloses that each channel is separately user-redefinable (See Column 4 Lines 28-33).

34. In reference to Claim 11, Burrus discloses the limitations as applied to Claim 7 above. Burrus further discloses that the at least one channel configuration is user-redefinable with one of a plurality of available configuration types (See Column 4 Lines 28-41).

35. In reference to Claim 13, Burrus discloses the limitations as applied to Claim 7 above. Burrus further discloses that at least one channel's configuration has a user-redefinable a maximum data transfer size (See Column 24 Lines 5-22).

36. In reference to Claim 16, Burrus discloses the limitations as applied to Claim 7 above. Burrus further discloses that at least one channel's configuration is user-redefinable with respect to the number of channels through which data is communicated (See Column 4 Lines 28-41).

37. In reference to Claim 17, Burrus discloses the limitations as applied to Claim 7 above. Burrus further discloses that any number of boards can be used by the system (See Column 3 Line 53 – Column 4 Line 8), and thus the utility is user-redefinable with respect to the number of data processing boards within the apparatus.

38. In reference to Claim 18, Burrus discloses the limitations as applied to Claim 17 above. Burrus further discloses that the instrument can have fewer boards installed than the number of available boards slots (See Column 3 Line 53 – Column 4 Line 8),

and thus is user-redefinable to define a number of data processing boards for the apparatus that is larger than the number of data processing boards actually used by the apparatus.

39. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burrus as applied to Claim 7 above, and further in view of FOLDOC.

40. In reference to Claim 8, Burrus discloses the limitations as applied to Claim 7 above. Burrus does not disclose that the boards are VME boards and the bus is a VME bus. FOLDOC discloses the use of a VME bus and boards (See entries 'VMEbus' and 'Versa Module Europa').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Burrus with a VME bus and boards, resulting in the invention of Claim 8, because VME is a standardized bus that is widely used (See entry 'VMEbus' in FOLDOC) and has become a popular protocol in the computer industry (See entry 'Versa Module Europa' in FOLDOC).

41. Claims 14, 48, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burrus as applied to Claims 7 and 36 above, and further in view of US Patent Number 6,938,118 to Blixt et al. ("Blixt").

42. In reference to Claim 14, Burrus discloses the limitations as applied to Claim 7 above. Burrus does not disclose that at least one channel's configuration has a user-redefinable board memory allocation. Blixt teaches a channel configuration having a redefinable memory allocation (See Column 14 Line 66 – Column 15 Line 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Burrus with the redefinable memory allocation of Blixt, resulting in the invention of Claim 14, because buffering the data allows a maximum data transfer speed to be achieved and making the memory allocation redefinable allows channels having a large data flow to have a correspondingly larger area in the memory (See Column 14 Line 66 – Column 15 Line 10 of Blixt).

43. In reference to Claim 48, Burrus discloses the limitations as applied to Claim 36 above. Burrus does not disclose that defining the configuration further comprises allocating memory space to a channel. Blixt teaches a channel configuration having a redefinable memory allocation (See Column 14 Line 66 – Column 15 Line 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Burrus with the redefinable memory allocation of Blixt, resulting in the invention of Claim 48, because buffering the data allows a maximum data transfer speed to be achieved and making the memory allocation redefinable allows channels having a large data flow to have a

correspondingly larger area in the memory (See Column 14 Line 66 – Column 15 Line 10 of Blixt).

44. In reference to Claim 49, Burrus and Blixt disclose the limitations as applied to Claim 48 above. Burrus further discloses allocating a receive queue size for the channel (See Column 24 Lines 5-22). Blixt further discloses allocating a receive queue size for the channel (See Column 15 Lines 5-11).

45. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burrus as applied to Claim 7 above, and further in view of Applicant's Admitted Prior Art ("AAPA").

46. In reference to Claim 19, Burrus discloses the limitations as applied to Claim 7 above. Burrus does not disclose that the first data processing board, the second data processing board, and the bus are implemented in a helmet for a pilot. AAPA teaches that the Strike Helmet 21 has multiple data processing boards connected by a bus (See Page 2 Lines 25-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the helmet of AAPA with the system of Burrus, resulting in the invention of Claim 19, in order to allow the programmer to customize the operation for each communications channel to obtain maximum hardware performance (See Column 4 Lines 9-12 of Burrus).

47. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burrus as applied to Claim 36 above, and further in view of US Patent Number 6,222,537 to Smith et al. ("Smith").

48. In reference to Claim 53, Burrus discloses the limitations as applied to Claim 36 above. Burrus does not disclose that the defining step further comprises defining the channel configurations according to data entry by a user via a graphical user interface. Smith teaches the use of a graphical user interface for inputting data into a computer (See Column 1 lines 10-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Burrus using the GUI of Smith, resulting in the invention of Claim 53, because GUI's are easy to use and do not require the user to know specific commands, operators, syntax rules, and the like (See Column 1 Lines 10-16 of Smith).

49. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burrus as applied to Claim 63 above, and further in view of Microsoft Press Computer Dictionary, Second Edition ("Microsoft").

50. In reference to Claim 64, Burrus discloses the limitations as applied to Claim 63 above. Burrus does not disclose that the user interface is a UNIX command line

interface. Microsoft discloses that the use of a UNIX command line interface is well known in the art (See entry 'UNIX').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Burrus with a UNIX command line interface, resulting in the invention of Claim 64, because UNIX is a powerful operating system that is more portable than other operating systems (See entry 'UNIX' in Microsoft).

Claim Objections

51. Claims 10, 11, 12, 13, 14, 16, and 18 are objected to because of the following informalities: The aforementioned claims all have a dependency upon cancelled Claim 9. For the purposes of evaluating prior art, the Examiner will interpret the claims to have a dependency upon Claim 7. Appropriate correction is required.

Allowable Subject Matter

52. Claims 20-22, 25-33, and 54-62 are allowed.

53. Claims 12 and 38-46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

54. The following is a statement of reasons for the indication of allowable subject matter: The Examiner can find neither prior art as a whole, nor motivation to combine the prior art, which discloses all of the limitations of Claims 12, 20-22, 25-33, 38-46, and 54-62. The prior art does not disclose the configuration types as claimed in Claims 12, 20-22, 25-33, 38-46, and 54-62 and defined in the Specification and Drawings.

Response to Arguments

55. Applicant's arguments with respect to Claims 1-8, 10-11, 13-14, 16-19, 34, 36-37, 47-53, and 63-66 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

56. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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